The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claims 1-13 (Cancelled)

14. (Currently Amended) A semiconductor device, comprising:

a semiconductor substrate having a semiconductor substrate main unit and a thin portion, the semiconductor substrate having a first surface that is planar and extends continuously along both the main unit and the thin portion, the thin portion being thinner than the semiconductor substrate main unit such that a recessed portion is formed in the semiconductor substrate at the thin portion, the thin portion having at least one through hole formed therein; and

a through wiring including a first wiring formed on [[a]] the first surface of the semiconductor substrate, a second wiring formed on a second surface opposite to the first surface, and a third wiring that fills the through hole, is formed along a wall surface of the recessed portion, and connects the first wiring and the second wiring,

the first wiring having a first sub-wiring extending from the main unit to the thin portion on the first surface of the semiconductor substrate in a direction perpendicular to a boundary between the main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending parallel to the boundary between the main unit and thin portion.

15. (Cancelled)

16. (Currently Amended) The semiconductor device according to claim 14 further comprising:

another semiconductor substrate disposed under the semiconductor substrate;

a third semiconductor element formed on a first surface of the another semiconductor substrate ~~facing the semiconductor substrate~~, the third semiconductor element having a gate

electrode, a source electrode, and a drain electrode, the first surface of the another semiconductor substrate facing second surface of the semiconductor substrate,

wherein the through wiring of the semiconductor substrate is connected to at least one of the source electrode and the drain electrode of the third semiconductor element.

17. (Cancelled)

18. (Currently Amended) The semiconductor device according to claim 14, wherein

~~the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and~~

the through hole being formed at a location corresponding to a connection part of the first sub-wiring and the second sub-wiring.

19. (Currently Amended) The semiconductor device according to claim 14, wherein

~~the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and~~

the through hole being formed at an end part of the second sub-wiring.

20. (Currently Amended) The semiconductor device according to claim 14, wherein

~~the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin~~

~~portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and~~

a plurality of the through holes formed under the second sub-wiring.

21. (Currently Amended) The semiconductor device according to claim 14, wherein

~~the first wiring has a first sub-wiring extending from the semiconductor substrate main unit to the thin portion on the first surface of the semiconductor substrate along a direction intersecting with a border of the semiconductor substrate main unit and the thin portion, and a second sub-wiring connected to the first sub-wiring and extending along the border on the thin portion, and~~

~~———~~[[a]] the third wiring is formed on the wall surface of the recessed portion along a direction intersecting with the border.

22. (Cancelled)